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EXAMINER	
SHERMAN, STEPHEN G	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/717,917	TSUBATA ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11,13,14,16,17 and 19-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11,13,14,16,17 and 19-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed the 24 May 2007. Claims 1 and 3-11, 13-14, 16-17 and 18-35 are pending. Claims 2, 12, 15 and 18 have been cancelled.

Response to Arguments

2. Applicant's arguments filed 24 May 2007 with respect to claims 1 and 3-11, 13-14, 16-17 and 18-34 have been fully considered but they are not persuasive.

With respect to the amendment made to claim 1 regarding the 112, 2nd paragraph rejection, the amendment to the claim is not enough to overcome the rejection. The applicant is merely reciting the same thing as recited previously just in a different way, and thus the rejection is maintained.

On page 12 of the applicants' response the applicants "vigorously traverse" the prior art rejections. The applicant states that JP 07-128685 would suggest that the black matrix of the prior art would be made into a conductor. The applicant then states that JP 07-128685 seeks to solve display problems by providing uniform storage capacitance and that there is no specific mention or suggestion in the reference of a gap for preventing parasitic capacitance between a pixel electrode and source line. The examiner respectfully disagrees. The examiner was only applying the reference to teach of a gap in the vertical direction, which Drawing 2 of the reference clearly shows.

It is not necessary for the reference to solve the same problem as the applicant's invention as long as the reference has the same structure. It is only what the reference would suggest to one of ordinary skill in the art, and Drawing 2 of the reference would suggest for someone to add a gap. Furthermore, the insulating property of the light shielding film is not essential to the applicant's invention since the applicant previously claimed in claims 12, 15 and 18 that the light shielding film was metal, i.e. a conductor.

The applicant is reminded that the rejection is based upon a COMBINATION of references. Mutsumi was used to teach of a gap and NOT that the black matrix is conductive. One cannot shown non-obviousness by attacking references individually where, as here, the rejections are based upon a combination of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The applicant continues the arguments on the bottom of page 5 by reciting paragraphs from the reference that relate to Drawings 6 and 7 of JP 07-128685, however, the examiner notes that these Drawing were NOT used in the rejection. Drawing 2 was used in the rejection, and therefore any mention to these drawings is irrelevant to the rejection.

The applicant then argues on page 13 that the office action makes an impermissible leap in hindsight in concluding that gap size or overlap size would be a matter of optimization. The examiner respectfully disagrees. The reference already teaches a gap, and it would be a matter of optimization to make is a certain width.

Claim Objections

3. Claims 6, 8,10, 13 and 16 is objected to because of the following informalities: Claims 6, 8, 10, 13 and 16 recite the limitation of "a light shielding film," however, claim 1 was previously amended to have the light shielding film limitation already claimed, so instead of reciting "a light shielding film" in claim 4, "the light shielding film" should be claimed.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 states the limitation: "the gap provided between the signal line and the pixel electrode is covered only by a layer(s) having an insulating property, at least one of the layers covering the gap including..." This limitation is indefinite because it is unclear as to whether the claim intends for there to only be one layer in view of the

vertical direction through the gap or whether the claim intends for there to be two layers in view of the vertical direction, one being the insulating layer and one being the light shielding film, i.e. black matrix. Furthermore, Figures 1, 3 and 4 of the applicant's specification show that there are multiple layers in view of the vertical direction and not just a layer. Therefore, it is unclear whether the specification is correct and the claim is wrong or whether the claim is right and the specification is wrong. For the purposes of examination, the examiner will assume that the Figures are correct and there is indeed multiple layers, not just one layer, in view of the vertical direction.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1, 4, 6, 8, 10, 13, 16, 19-22 and 24-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA (Page 1, line 8, to page 9, line 2 of the specification and Figures 12 and 13) in view of Matsuo (JP 07-128685).

Regarding claim 1, AAPA discloses a display device substrate (Figure 13, item 110), comprising:

one or more pixel electrodes each of which is provided on each intersection of a signal line and a scanning line that are provided on an insulating substrate (Figures 12 and 13 show that pixel electrode 103' is located at the intersection of scanning line 104 and a signal line 102, and are provided on substrate 110, which it explained to be insulating on page 5, lines 16-20.); and

an interlayer insulating film stacked between the signal line and the pixel electrode (Figure 13 shows interlayer insulating film layer 115 between the signal line 102 and the pixel electrode 103'.),

wherein in view of a vertical direction with respect to the surface of the insulting substrate, only a layer(s) having an insulating property is provided between the signal line and the pixel electrode (Figure 13 shows that only layer 115 is between pixel electrode 103' and signal line 102, where page 6, lines 16-17 explain that layer 115 is an insulating layer.), at least one of the layers including a light shielding film having an insulating property (Figure 13 shows that layer 115 includes light shielding film 108, and is explained to having an insulating property on page 6, lines 4-9.).

AAPA fails to teach that in view of a vertical direction with respect to a surface of the insulating substrate, the signal line is provided on an area on which the pixel electrode is not provided, and a gap is provided between the signal line and the pixel electrode.

Matsuo discloses a display device substrate (Drawing 2, substrate 9) where in view of a vertical direction with respect to a surface of the insulating substrate, the signal line is provided on an area on which the pixel electrode is not provided, and a gap is provided between the signal line and the pixel electrode (Drawings 1 and 2 shows that there is a gap between the signal lines 2 and the pixel electrode 3.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to provide a gap between the signal line and the pixel electrode as taught by Matsuo with the substrate structure taught by AAPA in order to reduce capacitive coupling of a pixel electrode and a source that causes unevenness and crosstalk of the vertical direction.

Regarding claim 4, AAPA and Matsuo disclose the display device substrate as set forth in claim 1.

Matsuo also discloses a display device substrate further comprising:

an active element provided on each intersection of the signal line and the scanning line (Drawings 1 and 2 and paragraphs [0003] and [0011] explain that the active region 10 is provided at a junction between the scanning lines 1 and signal lines 2.);

the light shielding film provided so as to cover at least a surface of the signal line among the signal line, the active element, and the scanning line (Drawings 1 and 2 show that light shielding film 8 covers the signal lines 2, the active element 10 and the scanning line 1.), wherein

in view of the vertical direction with surface of the insulating substrate, respect to the a gap between the pixel electrodes which are adjacent to each other with the signal line there between is covered by the light shielding film (Drawings 1 and 2 show that the gap between the pixel electrode 3 is covered by the light shielding film 8.).

Regarding claim 6, AAPA and Matsuo disclose the display device substrate as set forth in claim 1.

Matsuo also disclose a display device substrate further comprising:

an active element provided on each intersection of the signal line and the scanning line (Drawings 1 and 2 and paragraphs [0003] and [0011] explain that the active region 10 is provided at a junction between the scanning lines 1 and signal lines 2.); and

the light shielding film provided so as to cover at least a surface of the signal line among the signal line, the active element, and the scanning line (Drawings 1 and 2 show that light shielding film 8 covers the signal lines 2, the active element 10 and the scanning line 1.), wherein

in view of the vertical direction with respect to the surface of the insulating substrate, (i) the light shielding film which covers the surface of the signal line film and

(ii) the pixel electrode overlap with each other (Drawings 1 and 2 show that the pixel electrodes 3 and the light shielding film 8 overlap each other.).

Regarding claim 8, AAPA and Matsuo disclose the display device substrate as set forth in claim 1.

Matsuo also discloses a display device substrate further comprising:

an active element provided on each intersection of the signal line and the scanning line (Drawings 1 and 2 and paragraphs [0003] and [0011] explain that the active region 10 is provided at a junction between the scanning lines 1 and signal lines 2.);

a contact hole for allowing the active element and the pixel electrode to be in contact with each other (Drawings 1 and 2 show that a contact hole electrically connects active portion 10 to pixel electrode 3, as explained in paragraphs [0003] and [0011].); and

a light shielding film provided so as to cover surfaces of the active element, the signal line, and the scanning line (Drawings 1 and 2 show that light shielding film 8 covers the signal lines 2, the active element 10 and the scanning line 1.), wherein

in view of the vertical direction with respect to the surface of the insulating substrate, (i) the light shielding film which covers the surface of the signal line film and (ii) the pixel electrode overlap with each other (Drawings 1 and 2 show that the pixel electrodes 3 and the light shielding film 8 overlap each other.).

Regarding claim 10, AAPA and Matsuo disclose the display device substrate as set forth in claim 1.

Matsuo also disclose a display device substrate further comprising:

an active element provided' on each intersection of the signal line and the scanning line (Drawings 1 and 2 and paragraphs [0003] and [0011] explain that the active region 10 is provided at a junction between the scanning lines 1 and signal lines 2.);

a contact hole for allowing the active element and the pixel electrode to be in contact with each other (Drawings 1 and 2 show that a contact hole electrically connects active portion 10 to pixel electrode 3, as explained in paragraphs [0003] and [0011].); and

a light shielding film provided so as to cover at least a surface of the signal line among the signal line, the active element, and the scanning line (Drawings 1 and 2 show that light shielding film 8 covers the signal lines 2, the active element 10 and the scanning line 1.), wherein;

the interlayer insulating film is a stacking body of two or more layers, and the light shielding film is stacked between an uppermost layer and a lowermost layer that constitute the made interlayer insulating film (Drawings 1 and 2 show that the interlayer insulating film is made of layers 12, 13 and 14, where the light shielding film is stack between the uppermost layer 14 and a lowermost layer 12.), and

in view of the vertical direction with respect to the surface of the insulating substrate, a gap between the pixel electrodes which are adjacent to each other with the

signal line there between is covered by the light shielding film (Drawings 1 and 2 show that the gap between the pixel electrode 3 is covered by the light shielding film 8.).

Regarding claim 13, AAPA and Matsuo disclose the display device substrate as set forth in claim 1.

Matsuo also discloses a display device substrate further comprising:

an active element provided on each intersection of the signal line and the scanning line (Drawings 1 and 2 and paragraphs [0003] and [0011] explain that the active region 10 is provided at a junction between the scanning lines 1 and signal lines 2.);

a contact hole for allowing the active element and the pixel electrode to be in contact with each other (Drawings 1 and 2 show that a contact hole electrically connects active portion 10 to pixel electrode 3, as explained in paragraphs [0003] and [0011].); and

a light shielding film provided so as to cover at least a surface of the signal line among the signal line, the active element, and the scanning line (Drawings 1 and 2 show that light shielding film 8 covers the signal lines 2, the active element 10 and the scanning line 1.), wherein:

the interlayer insulating film is a stacking body made of two or more layers, and the light shielding film is stacked between an uppermost layer and a lowermost layer that constitute the interlayer insulating film (Drawings 1 and 2 show that the interlayer

insulating film is made of layers 12, 13 and 14, where the light shielding film is stack between the uppermost layer 14 and a lowermost layer 12.), and

in view of the vertical direction with respect to the surface of the insulating substrate, (i) the light shielding film which covers the surface of the signal line film and (ii) the pixel electrode overlap with each other (Drawings 1 and 2 show that the pixel electrodes 3 and the light shielding film 8 overlap each other.).

Regarding claim 16, AAPA and Matsuo disclose the display device substrate as set forth in claim 1.

Matsuo also discloses a display device substrate further comprising:

an active element provided on each intersection of the signal line and the scanning line (Drawings 1 and 2 and paragraphs [0003] and [0011] explain that the active region 10 is provided at a junction between the scanning lines 1 and signal lines 2.);

a contact hole for allowing the active element and the pixel electrode to be in contact with each other (Drawings 1 and 2 show that a contact hole electrically connects active portion 10 to pixel electrode 3, as explained in paragraphs [0003] and [0011].); and

a light shielding film provided so as to cover surfaces of the active element, the signal line, and the scanning line (Drawings 1 and 2 show that light shielding film 8 covers the signal lines 2, the active element 10 and the scanning line 1.), wherein:

the interlayer insulating film is a stacking body made of two or more layers, and the light shielding film is stacked between an uppermost layer and a lowermost layer that constitute the interlayer insulating film (Drawings 1 and 2 show that the interlayer insulating film is made of layers 12, 13 and 14, where the light shielding film is stack between the uppermost layer 14 and a lowermost layer 12.), and

in view of the vertical direction with respect to the surface of the insulating substrate, (i) the light shielding film which covers the surface of the signal line film and (ii) the pixel electrode overlap with each other (Drawings 1 and 2 show that the pixel electrodes 3 and the light shielding film 8 overlap each other.).

Regarding claim 19, AAPA and Matsuo disclose the display device substrate as set forth in claim 1.

Matsuo also disclose wherein the gap is set to be within a range of from not less than 1μm to not more than 20μm (It would be inherent that the gap between the pixel electrode 3 and signal line 2 taught by Mutsumi would be within a range of from not less than 1μm to not more than 20μm.).

Regarding claim 20, AAPA and Matsuo disclose a liquid crystal display device, comprising the display device substrate as set forth in claim 1 (Paragraph [0001] of Matsuo).

Regarding claim 21, please refer to the rejection of claim 1, and furthermore it would be inherent that there are plural pixel electrodes.

AAPA and Matsuo fail to teach of a size of the gap being set to provide a desired $\Delta\Delta\beta$ value which is interrelated with display unevenness, however, since when a gap is introduced between the pixel electrodes and signal lines display unevenness is reduced, it would have been an obvious design choice to "one of ordinary skill" in the art at the time the invention was made to optimize the gap to a desired value to provide the best display characteristics possible.

Regarding claim 22, AAPA and Matsuo disclose a display device substrate as set forth in claim 21.

Matsuo also discloses a display device substrate further comprising a light shielding film provided over the signal line and the gap (Drawing 2, black matrix 8), the pixel electrode being provided over at least a portion of the light shielding film (Drawing 2 shows that pixel electrode 3 is provided over a portion of black matrix 8.).

Regarding clam 24, AAPA and Matsuo disclose the device substrate as set forth in claim 22.

Matsuo also discloses a display device substrate further comprising:

an active element provided on each respective intersection of the signal line and the scanning line (Drawings 1 and 2 and paragraphs [0003] and [0011] explain that the

active region 10 is provided at a junction between the scanning lines 1 and signal lines 2.);

wherein the light shielding film is provided so as to cover at least a surface of the signal line among the signal line, the active element, and the scanning line (Drawings 1 and 2 show that light shielding film 8 covers the signal lines 2, the active element 10 and the scanning line 1.).

Regarding claim 25, AAPA and Matsuo disclose a display device substrate as set forth in claim 22.

AAPA also disclose a display device substrate wherein the light shielding film covers a signal line associated with a first pixel electrode and is overlapped by a second pixel electrode (Figure 13 shows pixel electrode 103 and pixel electrode 103' respectively), the first pixel electrode being directly driven by the signal line and the second pixel electrode not being directly driven by the signal line (Pixel electrode 103 is connected to the drain and therefore is directly driven and since 103' is not connected it is not directly driven.).

Matsuo also disclose of a display device wherein an overlap of the second pixel electrode and the light shielding film having a width y (Drawing 2 shows that there is an overlap between the pixel electrode 3 and the black matrix 8 that has some width.).

AAPA and Matsuo fail to teach wherein y is not less than 0.6 μm and not more than 5 μm, however, it would have been an obvious design choice to "one of ordinary

skill" in the art at the time the invention was made to optimize the overlap to a desired width in order to provide the best display characteristics possible.

Regarding claim 26, AAPA and Matsuo disclose a display device substrate as set forth in claim 21, wherein the desired $\Delta\Delta\beta$ value is not more than 0.08 (It would be inherent that the value would be less than 0.08 in order to provide a optimal display.).

Regarding claim 27, AAPA and Matsuo disclose a display device substrate as set forth in claim 21.

AAPA also disclose wherein the interlayer insulating film comprises a stacking body, the stacking body comprising an upper interlayer insulating film and a lower interlayer insulating film (Figure 13 shows interlayer insulating film 115 and 111 which are stacked upon each other on the substrate 110.).

Regarding claim 28, AAPA and Matsuo disclose a display device substrate as set forth in claim 27.

AAPA and Matsuo fail to teach wherein the upper interlayer insulating film has a dielectric constant of about 3.7, however it would have been an obvious design choice to "one of ordinary skill" in the art at the time the invention was made to choose an insulating film with an optimized dielectric constant so as to provide for the best display characteristics possible depending on the characteristics of the other materials used.

Regarding claim 29, AAPA and Matsuo disclose a display device substrate as set forth in claim 27.

AAPA and Matsuo fail to teach wherein the upper interlayer insulating film has a thickness of about 2.5 μm, however it would have been an obvious design choice to "one of ordinary skill" in the art at the time the invention was made to optimize the thickness of the insulating layer to a desired thickness based upon the characteristics of the other materials in order to provide for the best display characteristics possible.

Regarding claim 30, AAPA and Matsuo disclose a display device substrate as set forth in claim 21.

AAPA and Matsuo fail to teach wherein the gap has a width in a range of not less than 1 μm and not more than 20 μm, however it would have been an obvious design choice to "one of ordinary skill" in the art at the time the invention was made to optimize the width of the gap to a desired value in order to provide for the best display characteristics possible.

Regarding claim 31, AAPA and Matsuo disclose a display device substrate as set forth in claim 21.

AAPA and Matsuo fail to teach wherein the pixel electrodes of the substrate are driven by a dot reversal driving system, however, it is well known in the art to drive liquid crystal displays by a dot reversal driving system.

Regarding claim 32, AAPA and Matsuo disclose a display device substrate as set forth in claim 21.

AAPA also discloses a display device substrate further comprising an active device associated with each pixel electrode (Figure 13 shows active element 114), the active device having a gate electrode (Figure 13 shows gate electrode 104) and at least part of a source electrode (Figure 13 shows source electrode 105), the pixel electrode being formed over a gate electrode and at least part of a source electrode of its associated active device (Figure 13 shows that the pixel electrode 103 is formed over the gate and source electrodes 104 and 105.).

Regarding claim 33, please refer to the rejection of claims 21-22, and furthermore AAPA also disclose a display device substrate wherein the light shielding film having an insulating property covers a signal line associated with a first pixel electrode and is overlapped by a second pixel electrode (Figure 13 shows pixel electrode 103 and pixel electrode 103' respectively), the first pixel electrode being directly driven by the signal line and the second pixel electrode not being directly driven by the signal line (Pixel electrode 103 is connected to the drain and therefore is directly driven and since 103' is not connected it is not directly driven.).

Matsuo also disclose of a display device wherein an overlap of the second pixel electrode and the light shielding film having a width y (Drawing 2 shows that there is an overlap between the pixel electrode 3 and the black matrix 8 that has some width.) and whereby a gap of width x is provided between the signal line and the pixel electrode

(Drawing 2 shows that there is a gap between the pixel electrode and the signal line that has some width.).

AAPA and Matsuo fail to teach wherein y is not less than 0.6 μm and not more than 5 μm and wherein x is in the rang of no less than 1 μm and not more than 20 μm, however, it would have been an obvious design choice to "one of ordinary skill" in the art at the time the invention was made to optimize the overlap and gap to desired widths in order to provide the best display characteristics possible.

Regarding claim 34, AAPA and Matsuo disclose a display device substrate as set forth in claim 33.

Matsuo also discloses a display device substrate further comprising:

an active element provided on each respective intersection of the signal line and the scanning line (Drawings 1 and 2 and paragraphs [0003] and [0011] explain that the active region 10 is provided at a junction between the scanning lines 1 and signal lines 2.);

wherein the light shielding film is provided so as to cover at least a surface of the signal line among the signal line, the active element, and the scanning line (Drawings 1 and 2 show that light shielding film 8 covers the signal lines 2, the active element 10 and the scanning line 1.).

Regarding claim 35, AAPA and Matsuo disclose a display device substrate as set forth in claim 21.

AAPA also discloses wherein the interlayer insulating film comprises a light shielding film having an insulating property (Figure 13 shows that layer 115 includes light shielding film 108, and is explained to having an insulating property on page 6, lines 4-9.).

9. Claims 3, 5, 7, 9, 11, 14, 17 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mutsumi (JP 07-128685) in view of Zhang et al. (US 6,396,470).

Regarding claims 3, 5, 7, 9, 11, 14, 17 and 23, AAPA and Matsuo disclose the display device substrate as set forth in claims 2, 4, 6, 8, 10, 13 and 16.

AAPA and Matsuo fail to teach wherein the light shielding film is made of resin having an insulating property.

Zhang et al. disclose of a light shielding film made of resin having an insulating property (Column 12, lines 54-63 explain that the light shielding film shown in Figure 8 is an insulating black resin.).

Therefore it would have been obvious to "one of ordinary skill" ion the art at the time the invention was made that the light shielding film taught by the combination of AAPA and Matsuo be made of an insulating resin as taught by Zhang et al. in order to allow the light shielding film to be forming in a desired area without using a resist mask.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

19 June 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER